CHAPTER-5

DESIGN OF A MAXIMUM POWER POINT TRACKER

5.1 Introduction

The maximum power point tracking (MPPT) circuit described in the previous chapter can be designed for a single photovoltaic (PV) panel or for a large array consisting of several panel; only the parameters will be changed.

Following is the description of the design procedure of the MPPT circuit for a single PV panel with the standard parameters.

5.2 Maximum Power Point tracker (MPPT) Circuit

The circuit diagram of a maximum power point tracker (MPPT) circuit is shown in Fig. 5.1. We are now going to discuss how this circuit works. This circuit comprises of *PV* array, analogue multiplier, differential amplifier, linear low frequency ramp generator, high frequency (audio) ramp generator, comparator, two stage transistor driver amplifier and a DC-TO-DC converter.

The PV array supplies power to the DC-TO-DC converter circuit through a low value resistance. The low valued resistance connected in series with the PV array terminal actually acts to sense the current flowing through the PV array terminals. A 0.5 ohm nicrome wire resistance was employed and the voltage developed across it therefore proportional to the current flowing this resistance (0.5 Ω).

The voltage across the low value resistance is connected to one input of a two input analogue multiplier; the other input is directly connected to the PV array positive terminal. These two voltage values are then multiplied by the analogue multiplier (AD734AN), the output of the analogue multiplier gives the power (V*I) supplied by the PV array.

The output voltage from the analogue multiplier, which indicates the power, is supplied to the differential amplifier (using 1C 741) for further voltage amplification.

The output of the 741 op-amp is applied to an analog differentiator circuit, which is constructed by an op-amp. When the power reaches its maximum value, the differentiator output

The differentiator output switches a MQSFET BF 256A ON and OFF. A constant current source along with a capacitor connected as shown in Fig. 5.1 acts as low frequency linear ramp generator. The ramp can be stopped increasing by the MOSFET switch.

Timer 555 IC is used as a audio frequency (20 KHz) ramp generator, where the transistor at the output of 555 IC acts as a buffer. The buffered ramp is applied to the non-inverting input of a comparator employed by a LM239D IC. The inverting input of the comparator is coupled to the low frequency ramp, as discussed earlier.

The output of the comparator is a PWM signal, whose duty cycle depends on the low frequency ramp applied to the inverting input. The PWM signal drives the transistor Q_2 of the Darlington connected DC-TO-DC converter, through the two stage driver amplifier, consisting of transistor Q_4 and Q_3.

The PWM signal applied to the power transistor Q_1 chops the PV array current. The chopped DC voltage is filtered by the inductor L, flywheel diode D and the capacitor C_2.

5.3 Design of A Maximum Power Point Tracker Circuit (MPPT):

PV array having the following characteristics may be used with the MPPT.

1. OPEN CIRCUIT VOLTAGE (V_{oc}) = 20 V
2. SHORT CIRCUIT CURRENT (I_{sc}) = 2.5 Amp.

The above values are at the highest insolation level (at noon) . Let the load (e.g. motor) be operating upto minimum insolation level of 25% of the highest value (IKW/m^2). At this insolation 2 (250 W/m^2), PV array should have the following electrical characteristics;

3. OPEN CIRCUIT VOLTAGE (V_{oc}) =15 V

A. SHORT CIRCUIT CURRENT (I_{sc}) =0.6 Amp.

The voltage to be maintained across the PV array under all circumstances is V_0 ,

V_0 =(20 + 15)V/2 =17.5 V

When the transistor Q_1 is ON (fig. 5.1), current I_{sc} = 2.5 Amp. passes through Q_1.
Transistor 2N3055A can be used a Q_1 which has the value of I_c higher than 2.5 Amp.

Base current I_1 is $$I_1 = \frac{I_{sc}}{\beta}.\gamma$$

Where, B = DC gain, Y = overdrive factor (4), I_1 = 2.5*4/20 = 0.5 Amp .

I_1 = 0.5 Amp. is the collector current of Q_2. Transistor BD135 wil work quite satisfactorily as Q_2.

Base current I_2 is needed for Q_2 is $$I_2 = \frac{I_1}{\beta}.\gamma$$

= 0.5*4/100

= 0.02 Amp.

So $I_2 = 20$ mA.

When Q_3 is OFF I_2 passes through R_1. The value of R_1 is therefore,

$$R_1 = \frac{V_0}{I_2}$$

$$= (17.5\text{-}0.6)/0.02$$

$$= 845\ \Omega$$

In place of 845 Ω, 1kohm ohms can be chosen.

So $R_1 = 1k\Omega$

2N3055A transistor can be used as Q_3. Low current also passes through Q_4, as 2N3055A can be chosen as Q_4 as well.

Base current I_3 for Q_3 is $$I_3 = \frac{I_2}{\beta}.\gamma$$

$$= 0.2*4/100$$

So $I_3 = 0.8$ mA.

I_3 will flow through R_3 during OFF time. The value of R_3 will be,

$$R_3 = \frac{V_0}{I_3}$$

$$= (17.5\text{-}0.6)/0.08$$

$$= 21.125\ K\Omega$$

Therefore $R_3 = 21\ K\Omega$ can be selected.

The base current I_4 needed for Q_4 is $$I_4 = \frac{I_3}{\beta}.\gamma$$

$$= 0.8*4/100 \qquad = 0.032 \text{ mA.}$$

The op-amp output could be +4V as maximum during high state, because the supply voltage is +4V.

The value of R_3 is $$R_3 = \frac{4 - V_{bc}}{I_4} \quad = (4\text{-}0.6)/0.032 \quad = 106\ K\Omega$$

So,R3=100KΩ can be chosen for the present circuit.

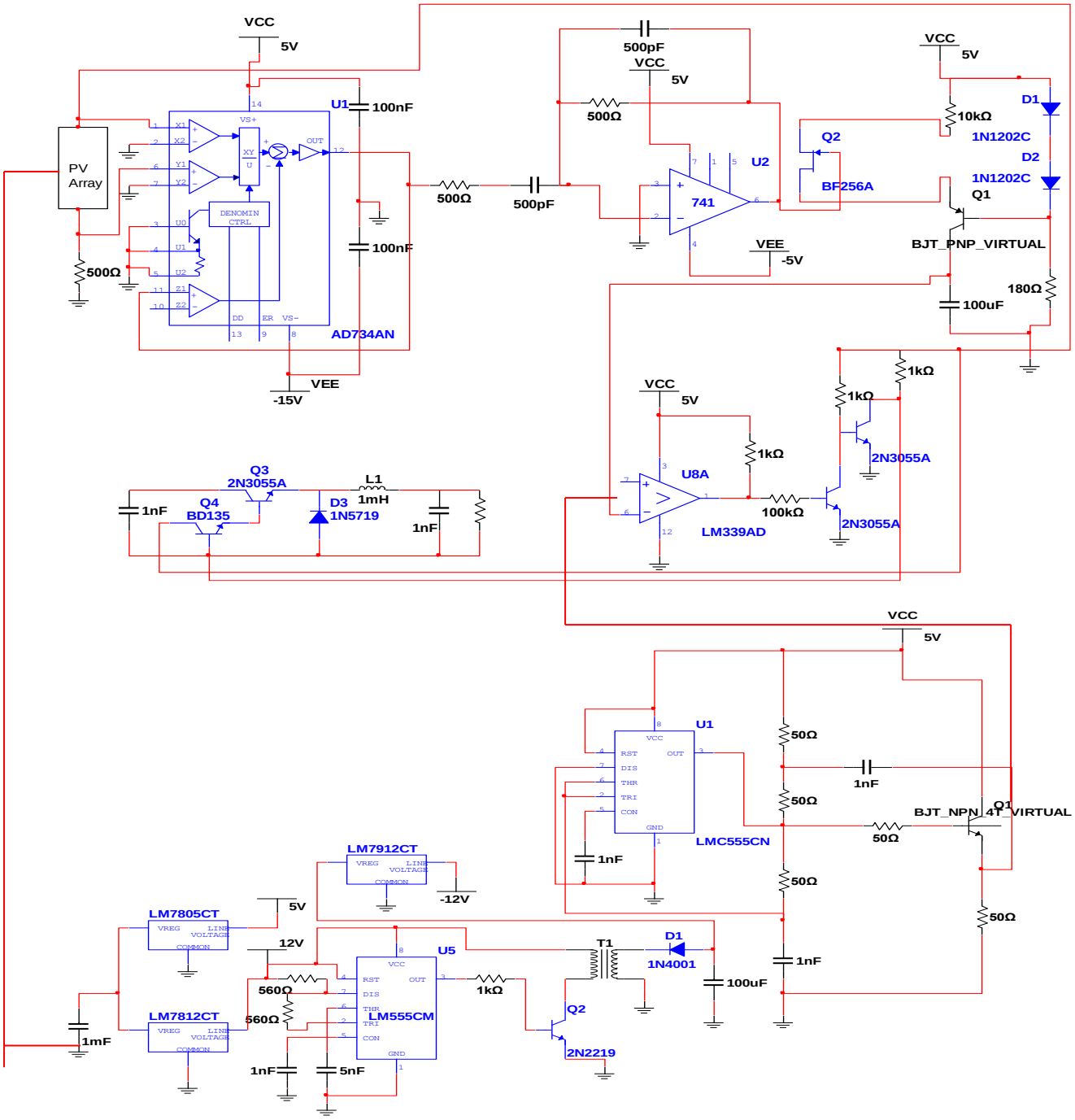

Fig: 5.1 Circuit Diagram of Maximum Power Point Tracker

5.4 Analogue Multiplier:

In this maximum power point tacking system , a two input analogue multiplier is used .This multiplier multiplies voltage and current values, giving power output value .Photovoltaic (PV) array voltage is applied at one input, PV current which is proportional to voltage across a low value resistance of PV array is applied at other input; the input of the multiplier givens an indication of the power delivered by the PV array.

The AD734AN general purpose analogue multiplier IC has been used. The output voltage is a linear function of two input voltages. The basic multiplier circuit is show in Fig (5.2) .The AD734AN is a monolithic, four quadrant analogue multiplier which operates on the principle of variable trans conductance .Hence the differential output current of the multiplier is given by, $W= (X_1-X_2) (Y_1-Y_2)/10V+Z_2$

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Let us assume that resistance dividers are used at the X and Y inputs to make 5.0 V for a 20V input (PV array open circuit voltage). If an overall scale factor of 1/10 is desired then

$$V_o = \frac{V_x' V_y'}{10} = \frac{4}{10} V_x V_y$$

Therefore, K =4/10 for the multiplier (excluding the divider network).The first step is to select current I_{x1} and current 1_{y1}.. I_{x1} and I_{y1} will normally be one or two milliamperes. Further Ix1 may or may not be equal to I_{y1}.

Let, $I_3 = I_{13} = 1$ Ma

At the input of the multiplier two capacitors of .1uF have been connected as shown in Fig. 5.2 to suppress 20 KHz ripple due to chopping.

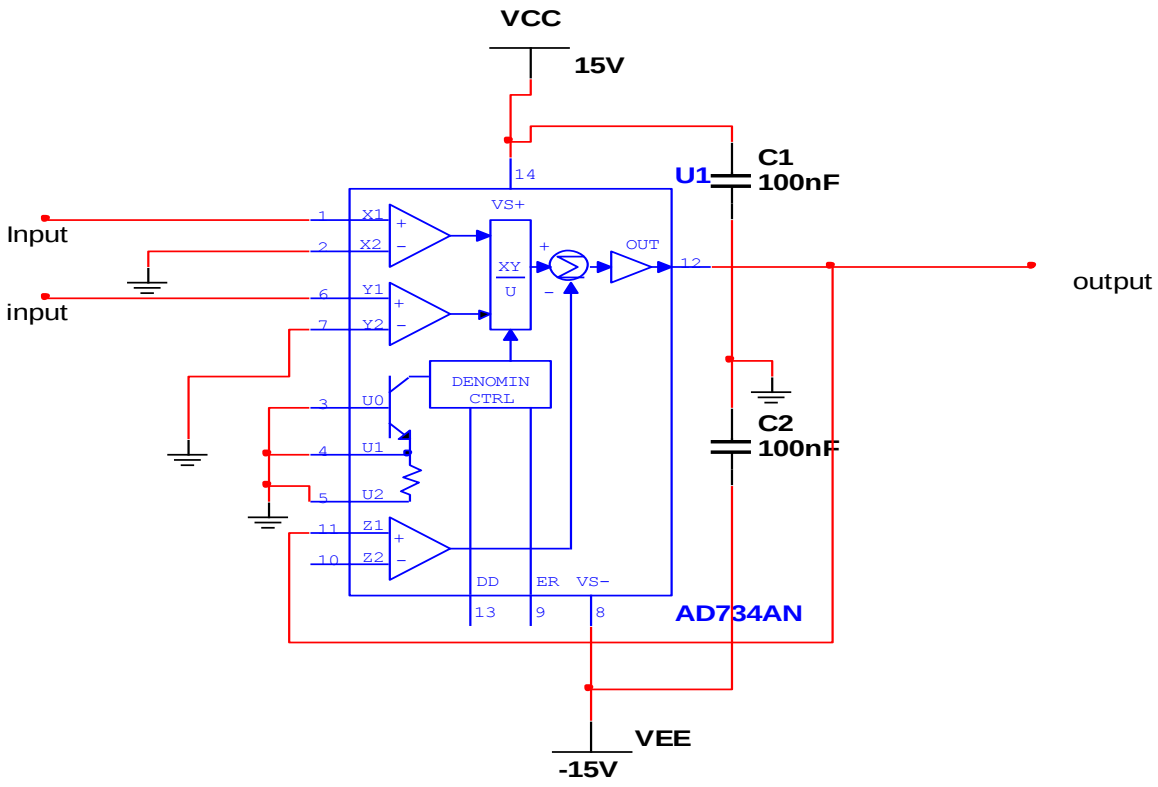
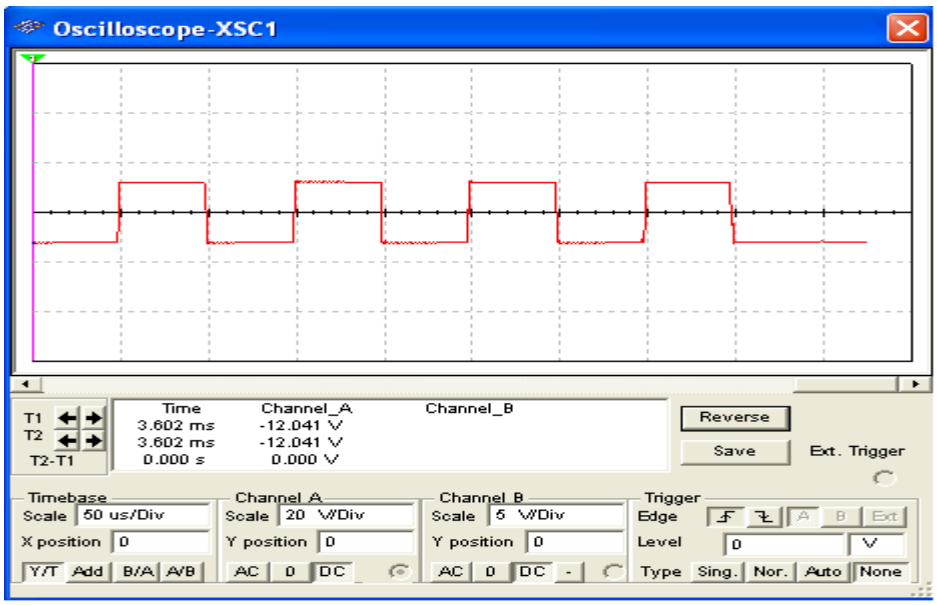


Fig 5.2 Analogue multiplier



5.5 Differentiator

An op-amp, in the configuration Fig (5.3) can be use as a differentiator. IC 741(single Op-amp) or IC 747 (dual Op-amp) can be used as a differentiator. In the letter case, one of two op-amps is used to implement. For the circuit Fig (5.3) considering the gain of the op-amp is very high (which is found in most of the practical case)

Therefore, $i_c = i_R$ ……..(1)

Here, $i_{c=C.\frac{dVi}{dt}}$ ……..……..…(2)

(Considering the inverting input as virtual ground)

And $i_{c=\frac{Vo}{R}}$ ……...(3)

From equation (1),(2)and(3), we get $\frac{V_o}{R} = C.\frac{dVi}{dt}$

Choosing, C1=500pF and R1=500Ω

So, $Vo=500 * 500\frac{dVi}{dt}$

Here,we use another resistance R2=500Ω which is in series with C1 and another capacitor C2=500pF which is in parallel with R1.

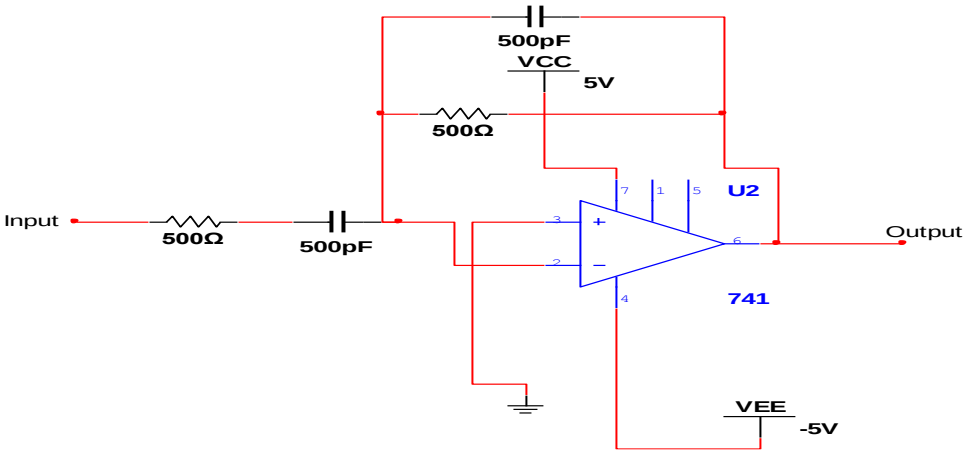
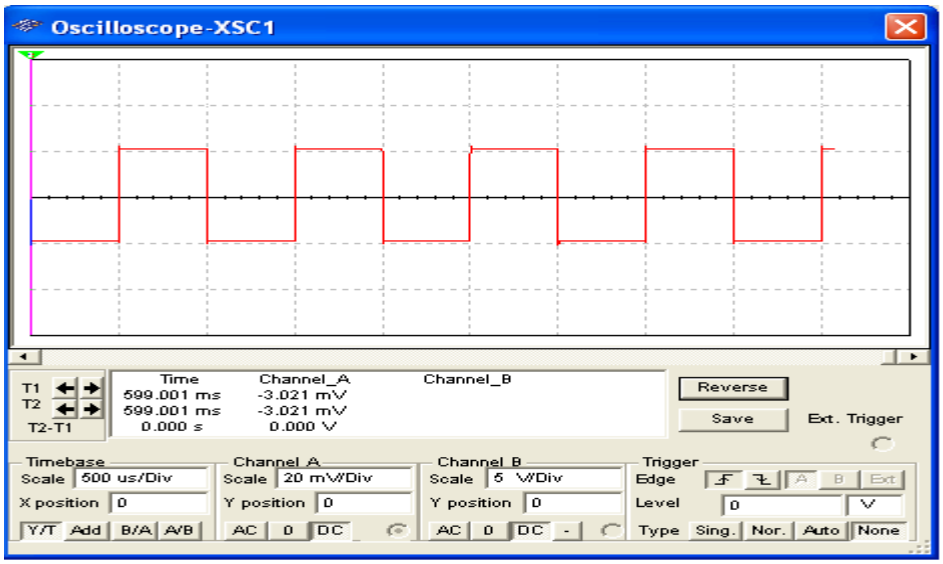


Fig 5.3 Differentiator



5.6 High Frequency (Audio) RAMP Generator

A continuous ramp signal is necessary to produce pulse width modulation (PWM) signal. The ramp signal is applied at the inverting input of comparator. The 555 timer IC can be used to generate temperature gradient saw-tooth waveforms (ramp) whose linearity is within 1%,using the circuit show in Fig(5.4)By connecting the timer's trigger and threshold inputs together ,it functions as the familiar astable.

Capacitor C_1 begins to charge through R_1, R_2 and R_3 towards V_{cc} (+5V). This change in voltage drives an emitter follower whose output is coupled back to the junction of R_1 and R_2 through capacitor C_2 for bootstrapping to achieve better linearity. Thus the voltage across R_2 essentially remains constant during the charging cycle of C_1, and produces the same effect of linear ramping as a constant current source feeding C_1.

555resets the timer's internal flip-flop, and the cycle repeated. Resistace R_3 is used to slow down the negative discharge slope of the saw-tooth. For proper operation, the following Once this linear saw-tooth signal at pin 6 reaches 2/3 V_{cc}, the internal comparator of 1C

relationships apply $R_1 = R_2$

$R_3C_1 > 10$ µsec

$R_1C_1 > 10. R_2C_2$

The saw-tooth frequency may be expressed as $f = \frac{1}{[0.75(R_1 + R_2) + 0.693R_3]C_1}$

Let the frequency of the ramp signal, f = 20 KHz Let us take the value of the capacitor, C_1 = 1 uF From the proper operation condition,

Saw-tooth frequency, $R_3C_1 > 10$ µsec

Let, $R_3C_1 = 50$ µsec

So R3 = 50 µsec/C1 = 50 µsec/1 µF = 50 Ω

Saw-tooth frequency, $f = \frac{1}{[0.75(R_1 + R_2) + 0.693R_3]C_1}$

$$20\ KHz = \frac{1}{[0.75(R_1 + R_2) + 0.693 \times 200]10.05uF}$$

Another condition for proper operation shows that $R_1 = R_2$

So, $$20\ KHz = \frac{1}{[0.75(2R_1) + 0.693 \times 200]10.05uF}$$

solving this equation we get, $R_1 = 50$ Ω,

$R_2 = 50$ Ω

and so $R_5 = 50$ Ω can be taken.

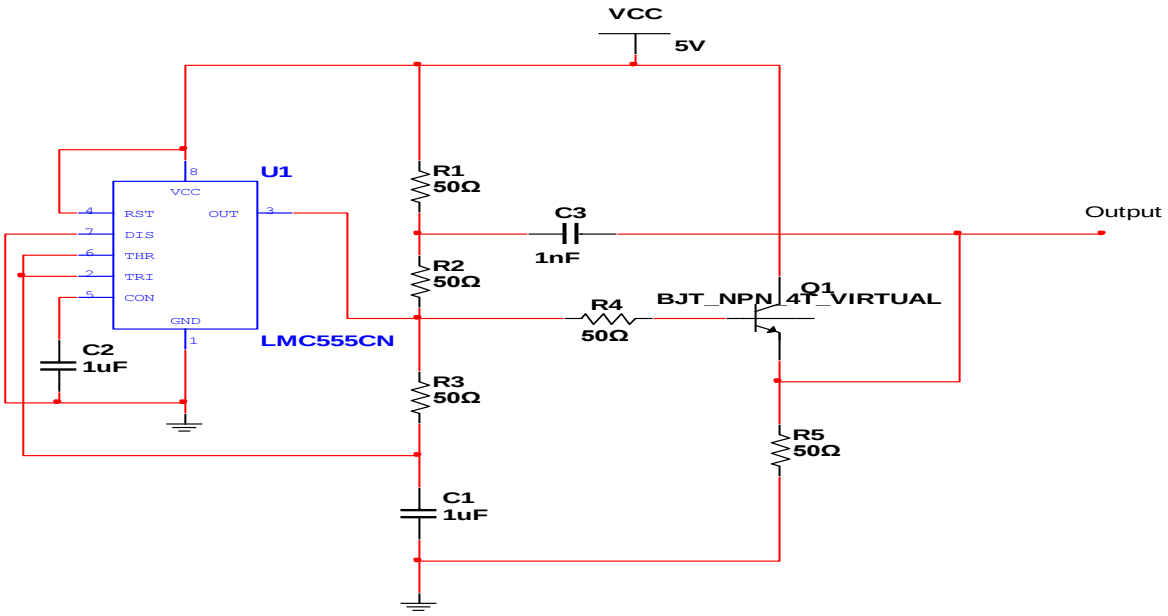
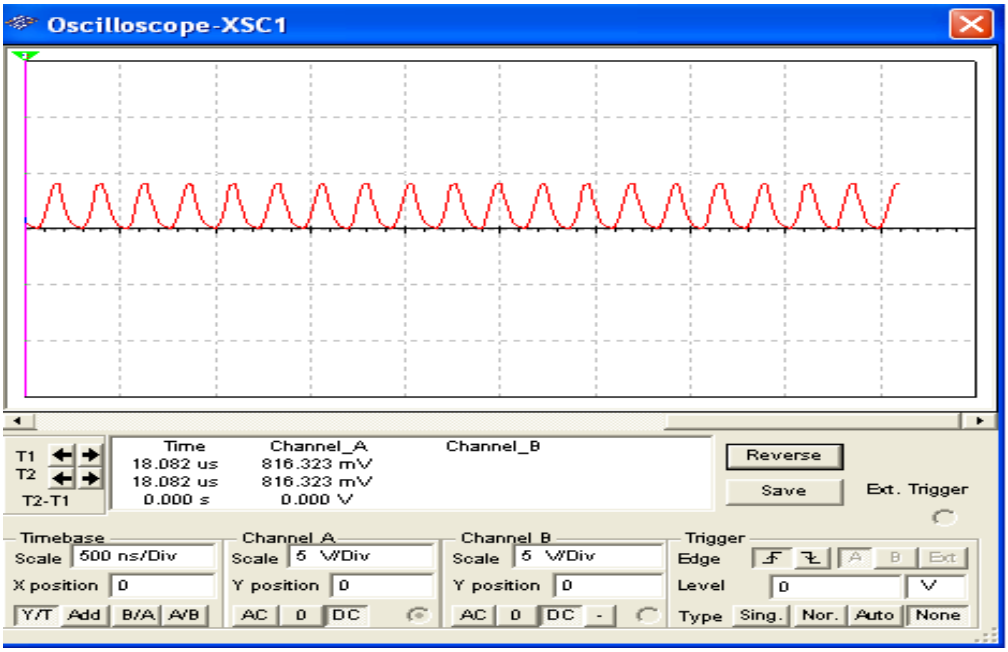


Fig 5.4 High Frequency Ramp Generator



5.7 Design of Linear (Low Frequency) RAMP Generator

A linear low frequency ramp generator circuit show in Fig(5.5)is used as a constant current source. When the capacitor C charges during the conducting period of the transistor, the voltage across the capacitor C increases linearly. This linear ramp is compared with high frequency (audio) ramp (from timer 555 IC) in the comparator to produce pulse width modulation(PWM).

The transistor in this circuit is PNP type and designated the number BJT PNP_ Virtual. The value of R and C is taken high to get large time constant. The diode 1N1202C are used which endure 1 amp current.

Choosing R = 10 KΩ

C = 100 µF

When the transistor conducts, there is a voltage drop of 0.6 volt between base and emitter of the transistor. Therefore the conducting current

i = 0.6/10 =60 µAmp is constant.

We know, when the capacitor charges, the charging current (which is the constant conducting current) is given by $i = c.\frac{dV_c}{dt}$,

$$\text{so } \frac{dV_c}{dt} = \frac{i}{c}$$

$$\text{Therefore, } V_c = \frac{1}{C}\int i dt$$

Since the charging current i is constant, i.e., i=I=60 µamp

So $$V_c = \frac{1}{C}\int dt = \frac{It}{C}$$

$$\Rightarrow t = \frac{It}{C}$$

Substituting the corresponding values in the above equation , i. e . ,

V_c = 12 volts

C =100 µF

I =60 µAmp

we get $$t = \frac{12 \times 100 \times 1^{-6}}{60 \times 10^{-6}} = 20 \text{sec}$$

Therefore the output goes to maximum of 12 volts after 20 seconds.

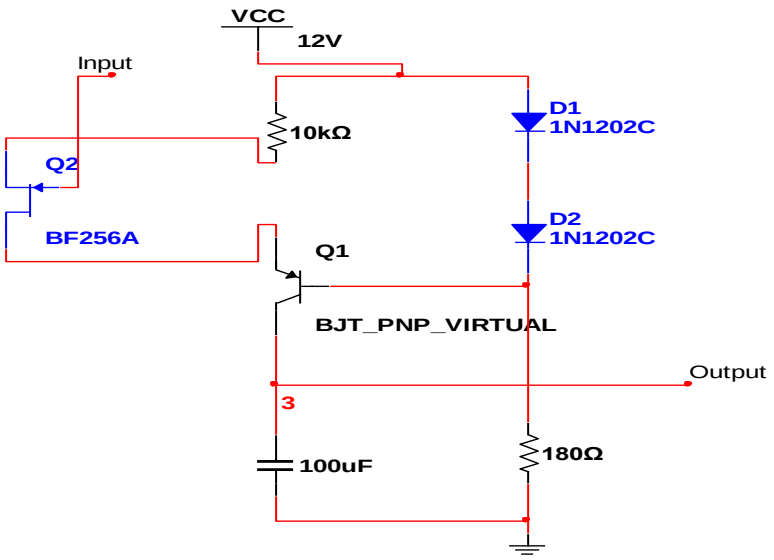
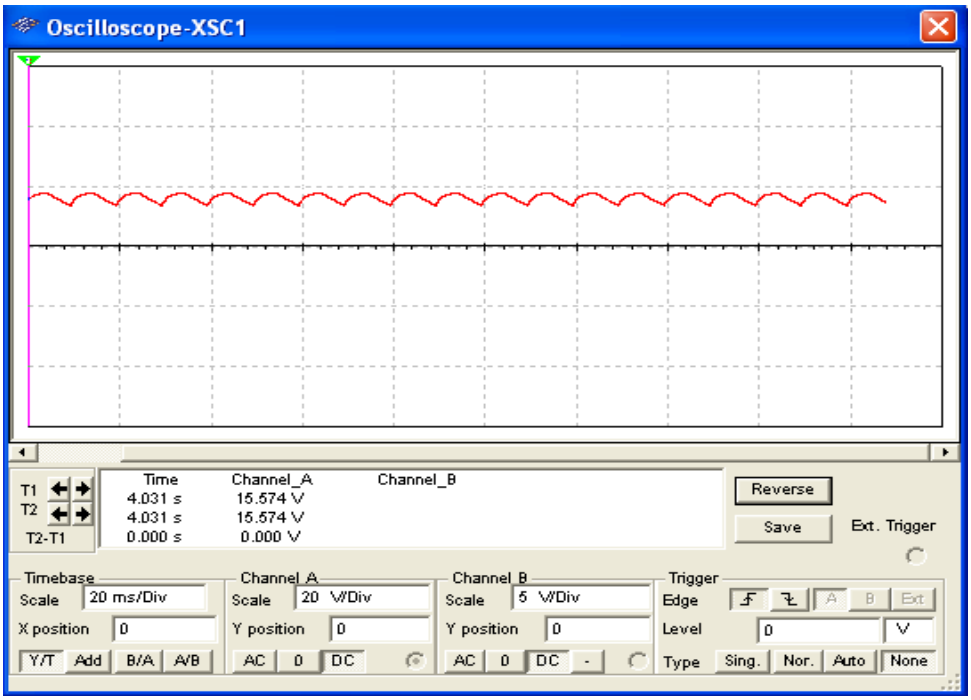


Fig 5.5 Linear Low Frequency ramp Generator



5.8 Comparator:

Operationa1 amplifier can be used to construct comparators. If a low frequency ramp is applied at the inverting terminal of the Op-Amp, the Op-Amp output will remain low as long as the non inverting point voltage is below the voltage applied at the inverting input ; the output voltage sharply rises when the non inverting point voltage just exceeds the voltage at the inverting point.

The output of the comparator is a series of square pulses whose width depends upon the linear(low frequency) ramp voltage. One Op-Amp of 1C LM239A can be used as this comparator *A* fig, 5.6). As the output of the Op-Amp is open collector, a pull-up resistance of IK is tied to -4-5 volts at the output of the Op-Amp. A +5 volts power supply is required for the operation of the Op-Amp.

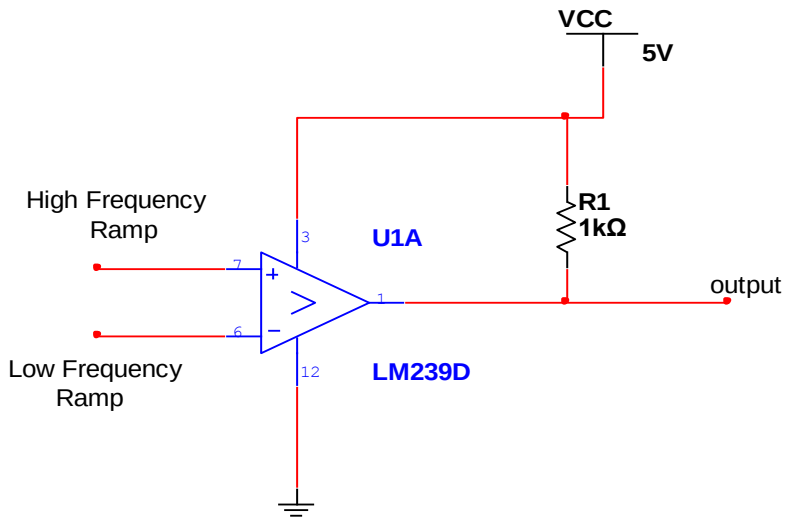


Fig 5.6 Comparator